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APPLICATION NO.	FILIN	G DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,441	02/04/2002		Jeffrey P. Kotowski	NSC1-G9800 [P05051]	7556
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Alfred A. Equitz				EXAMINER	
GIRARD & EQUITZ LLP				HUR, JUNG H	
Suite 1110 400 Montgomery Street					
San Francisco, CA 94104		4		ART UNIT	PAPER NUMBER
				2824	
				DATE MAILED: 04/23/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	(Applicant(s)	_/
•	10/067,441	KOTOWSKI ET AL.	
Office Action Summary	Examiner	Art Unit	
	Jung (John) Hur	2824	
The MAILING DATE of this communication a	appears on the cover sheet w	rith the correspondence address	
Period for Reply	NIVIO OET TO EVOIDE OF	AONTHO FROM	
A SHORTENED STATUTORY PERIOD FOR REF THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a - If NO period for reply is specified above, the maximum statutory peri - Failure to reply within the set or extended period for reply will, by stat - Any reply received by the Office later than three months after the ma earned patent term adjustment. See 37 CFR 1.704(b).	N. 1.136(a). In no event, however, may a reply within the statutory minimum of tho dwill apply and will expire SIX (6) MO tute, cause the application to become A	reply be timely filed rly (30) days will be considered timely. NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).	
Status 1) Recognitive to communication(s) filed on			
1) Responsive to communication(s) filed on _2a) This action is FINAL.2b) ≥	This action is non-final.		
,-		otters prosecution as to the morits is	
closed in accordance with the practice und			
Disposition of Claims			
4)⊠ Claim(s) <u>1-40</u> is/are pending in the applicat			
4a) Of the above claim(s) is/are withd	rawn from consideration.		
5) Claim(s) is/are allowed.			
6) Claim(s) <u>1-24,28-32 and 35</u> is/are rejected.			
7) Claim(s) <u>25-27,33,34 and 36-40</u> is/are object			
8) Claim(s) are subject to restriction and Application Papers	d/or election requirement.		
9)⊠ The specification is objected to by the Exami			
10) ☐ The drawing(s) filed on is/are: a) ☐ ac	cepted or b) objected to by	the Examiner.	
Applicant may not request that any objection to			
11) The proposed drawing correction filed on		disapproved by the Examiner.	
If approved, corrected drawings are required in	. •		
12) The oath or declaration is objected to by the	Examiner.	·	
Priority under 35 U.S.C. §§ 119 and 120		2.4.2.4.3.4.9.40	
13) Acknowledgment is made of a claim for fore	ign prionty under 35 U.S.C.	§ 119(a)-(d) or (t).	
a) All b) Some * c) None of:			
1. Certified copies of the priority docume			
2. Certified copies of the priority docume			
3. Copies of the certified copies of the p application from the International* See the attached detailed Office action for a I	Bureau (PCT Rule 17.2(a)).	•	
14) Acknowledgment is made of a claim for dome	estic priority under 35 U.S.C	. § 119(e) (to a provisional application)).
 a) The translation of the foreign language 15) Acknowledgment is made of a claim for dome 			
Attachment(s)			,
 Notice of References Cited (PTO-892) Dotice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449) Paper No(s 	5) Notice o	Summary (PTO-413) Paper No(s) Informal Patent Application (PTO-152) earch history .	<i>4</i> * * * * * * * * * * * * * * * * * * *

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DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it is more than 150 words in length, and the first sentence is incomplete. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the external node" in at least line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim. The limitation "at least one external node" in line 2 of the claim also claims more than one nodes; in such case, it is unclear which node "the external node" refers to. For the purpose of this examination, "the external node" in claim 1 and its dependent claims is understood as one same node of "at least one external node".

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In claim 1, it is unclear whether "a control signal" in lines 8-9 of the claim is a part of "at least one control signal" in lines 3-4 of the claim.

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Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 5. Claims 1 and 28, insofar as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Schneider et al. (U.S. Pat. Appl. Pub. No. 2002/0097616).

Regarding claims 1 and 28, Schneider in Figs. 1 and 2 discloses an integrated circuit and a method of testing the integrated circuit, comprising: at least one external node (21); operational circuitry (circuitry to be tested by BIST; see, for example, paragraphs 3 and 5) configured to operate in response to at least one control signal (clock); and test circuitry (BIST) coupled to the external node and the operational circuitry, wherein the test circuitry is configured to operate in at least one test mode in response to test data (C encoded in A in Fig. 2) received at the external node from an external source (1), and the test circuitry is configured to assert to the operational circuitry a control signal (B in Fig. 2) in response to an external control signal (clock signal encoded in A in Fig. 2) received at the external node.

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6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 2-6, 9, 21-24, and 29-32, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider et al. (U.S. Pat. Appl. Pub. No. 2002/0097616) in view of Knotz (U.S. Pat. No. 6,289,055).

Regarding claims 2, 21, and 29, Schneider discloses an integrated circuit and a method as in claims 1 and 28 above, and further discloses in Fig. 2 that the test circuitry is configured to extract the test data from a modulated input signal (signal A) asserted to the external node from the external source, and to generate the control signal in response to the input signal, with the exception of the modulated input signal being an amplitude-modulated input signal.

Knotz discloses an amplitude-modulated input signal (for example, signal m in Fig. 3).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the integrated circuit and the method of Schneider such that the input signal is an amplitude-modulated signal as in Knotz, since amplitude modulation is an alternative means of combining a plurality of signals, well-known in the art, and both references have the same objective of reducing the number of pins/leads (see Schneider, paragraph 5, and Knotz, column 1, lines 17-21).

Regarding claims 3, Schneider, in figure 2, and Knotz, for example in figure 3, further disclose that the external control signal is a binary signal determined by the input signal (clock

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from the external source encoded in the modulated input signal), and the test circuitry is operable in a mode in which the control signal (extracted clock) is a binary signal whose state is determined by the state of the external control signal (clock from the external source).

Regarding claims 4, 22, 30 and 31, Schneider, in figures 1 and 2, and Knotz, for example in figures 2 and 3, further disclose that the test circuitry is configured to extract a clock signal (B in Schneider, and SC' in Knotz) from the input signal, and to operate in response to the clock signal during said at least one test mode.

Regarding claims 5, 6, 23, 24, and 32, (3,4 levels, FFs), Knotz, for example in figures 2 and 3, further disclose that the input signal has at least three levels, including a low level (L) below a first threshold (V2), a high level (H2) above a second threshold (V1), and an intermediate level (H1) between the first threshold and the second threshold, and wherein the test circuitry includes: first comparator circuitry (32), coupled to receive the input signal and configured to operate in a first mode in which said first comparator circuitry generated a first signal (SC') indicative of whether the input signal has a level less than the first threshold, second comparator circuitry (31), coupled to receive the input signal and configured to operate in a first mode in which said second comparator circuitry generates a second signal (S31) indicated of whether the input signal has a level greater than the second threshold; and a flip-flop (6) having a set terminal (S), a reset terminal (C), and an output (Q), wherein the set terminal is coupled to receive the second signal, the reset terminal is coupled to receive the first signal, the output asserts a data signal (SD') in response to the first signal and the second signal, and the data

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signal is indicative of the test data (SD' is a regenerated data signal; see, for example, column 3, line 65 through column 4, line 4).

Regarding claim 9, Knotz, for example in Figs. 6, 7, and 10, further discloses that the test circuitry includes a comparator circuitry (for example, 30) coupled and configured to receive the input signal, to extract the test data (SD') from the input signal, and to extract a latch signal (EN') from the input signal, wherein the latch signal is indicative of whether the input signal has a level exceeding a latch threshold (V3); and at least one register (R) coupled to the comparator circuitry for receiving the latch signal and at least some of the test data (SD').

8. Claims 14, 15, and 35, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider et al. (U.S. Pat. Appl. Pub. No. 2002/0097616) as applied to claims 1 and 28 above, and further in view of Kato (U.S. Pat. No. 5,557,571).

Regarding claims 14, 15, and 35, Schneider discloses an integrated circuit and a method as in claims 1 and 28 above, with the exception of the test circuitry configure to assert data to the external node, for transmission to external circuitry during a measurement mode. Kato discloses a circuitry configure to assert signal to the external node during a measurement mode (see, for example, column 5, lines 17-30 with reference to Figs. 1 and 7). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the test circuitry of Schneider in view of Kato to assert data to the external node during a measurement mode, for the purpose of not having to provide an extra pin for such function (Kato, for example, column 5, lines 14-16).

9. Claims 25-27, 33, 34, and 36-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- 10. Claims 7, 8, 10-13, and 16-20, insofar as understood, would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
- The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 7, 16, and 36, the prior arts of record do not disclose or suggest an integrated circuit or a method including a means to terminate a test mode based on the level of an input signal remaining below a first threshold for a predetermine minimum time or the frequency of the data bits being less than a predetermined minimum frequency.

Regarding claims 8 and 25, the prior arts of record do not disclose or suggest an integrated circuit wherein an input signal has at least four levels, including a latch level above a third threshold, where the third threshold is greater than a second threshold.

Regarding claim 10, 13, 26, 27, and 33, the prior arts of record do not disclose or suggest an integrated circuit or a method including a nonvolatile memory comprising at least one programmable cell having a first input coupled to receive a sequence of bits of the test data received at the external node.

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Regarding claims 17 and 38, the prior arts of record do not disclose or suggest an integrated circuit or a method including a lock circuitry operable to analyze data to determine whether said test data is indicative of a digital key, and to generate a second control signal in response to determining that said test data is indicative of the digital key.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (703) 308-1624. The examiner can normally be reached on M-Th 6:00 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jhh April 16, 2003

> Vu A. Le Primary Examiner